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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,732	SUGURO ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 34-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 34-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/609,107.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 3-5, 34 and 37-39 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Fig. 12 discloses the element isolating insulating film [62] having a top surface projecting upward above a top surface of the semiconductor layer [61]. It further discloses the top surface position of said element isolating insulating film [62] is not higher than a top surface position of the gate electrode [64]. However, the specification never discloses said gate insulating film being formed on a top surface and sides of the semiconductor layer in said element regions which are not covered with said element isolating insulating film as claimed in claims 3, 38 and 39 and in fig. 12.

2. Claims 1-4 are objected to because of the following informalities: Claim 1, lines 13-14, the phrase "the top surface position of said element isolating insulating film" and line 14, the phrase "the top surface position of said semiconductor layer" have no antecedent basis. Claim 2, lines 12-13, the phrase "the top surface position of said element isolating insulating film", line 13, the phrase "the top surface position of said semiconductor layer" and line 15, the phrase "the gate electrode" have no antecedent basis. Claim 3, line 15, the phrase "the top surface position of said element isolating insulating film" has no antecedent basis. Claim 4, lines 2-3, the phrase "the top surface position of said semiconductor layer" has no antecedent basis. Appropriate correction is required.

3. Claims 1-5 and 34-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 17-19, claim 2, lines 15-17, claim 3, lines 16-18, the phrase "said element isolating insulating film and said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer" is vague and indefinite. Fig. 1D discloses said element isolating insulating film [2] and each of said element regions [3] make an interface which is substantially perpendicular to the top surface of said semiconductor layer [1]. Claims 1-3 should rewrite as "said element isolating insulating film and each of said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer".

Claim 3, lines 12-14, the phrase "said gate insulating film is formed on a top surface and sides of the semiconductor layer in said element regions which are not covered with said element isolating insulating film" is vague and indefinite. Fig. 19B discloses said gate insulating film [73] is formed on a top surface and sides of the semiconductor layer [71] in each of said element regions which is not covered with said element isolating insulating film [72]. Claim 3 should rewrite as "said gate insulating film is formed on a top surface and sides of the semiconductor layer in each of said element regions which is not covered with said element isolating insulating film.

Claim 38, lines 3-5, claim 39, lines 3-5, the phrase "said gate insulating film being formed on a top surface and sides of the semiconductor layer in said element regions which are not covered with said element isolating insulating film" is vague and indefinite.

Fig. 19B discloses said gate insulating film [73] being formed on a top surface and sides of the semiconductor layer [71] in each of said element regions which is not covered with said element isolating insulating film [72]. Claims 38 and 39 should rewrite as "said gate insulating film being formed on a top surface and sides of the semiconductor layer in each of said element regions which is not covered with said element isolating insulating film.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 35 and 36 insofar, as in compliance with 35 USC 112, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yamazaki.

In regards to claim 1, Yamazaki shows all the elements of the claimed invention in fig. 8F. It is a semiconductor device, comprising: a substrate [101] having a semiconductor layer [103] and a trench (the area occupied by the lower portion of the oxide film [110]), said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions; an element isolating insulating film [110] provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a surface of said semiconductor layer; wherein the element isolating insulating film [110] is an oxide film; and a MOS type element formed within a corresponding one of the element regions and having a gate insulating film [118] and a

gate electrode [122a] on the gate insulating film [118], wherein: a difference in height from the substrate between a top surface position of said element isolating insulating film and a top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film, the top surface position of said element isolating insulating film [110] is not higher than a top surface position of the gate electrode [122a], and said element isolating insulating film [110] and each of said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer.

In regards to claim 2, Yamazaki shows all the elements of the claimed invention in fig. 8F. It is a semiconductor device, comprising: a substrate [101] having a semiconductor layer [103] and a trench (the area occupied by the lower portion of the oxide film [110]), said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions; an element isolating insulating film [110] provided in the trench for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film having a top surface projecting upward above a top surface of the semiconductor layer; wherein the element isolating insulating film [110] is an oxide film; and a MOS type element formed within a corresponding one of said element regions and having a gate insulating film [118], wherein: a difference in height from the substrate between a top surface position of the element isolating insulating film [110] and a top surface position of the semiconductor layer is at least 10 nm because the height of the top portion of the insulating film [110] is larger than the thickness of the gate insulating film [118] (col. 15, lines 10-14). It further

discloses the top surface position of said element isolating insulating film [110] is not higher than a top surface position of a gate electrode [122a], and said element isolating insulating film [110] and each of said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer.

In regards to claims 35 and 36, Yamazaki further discloses said element isolating insulating film [110] is a thermally grown oxide film (LOCOS oxide film).

6. Applicant's arguments filed 4/1/05 have been fully considered but they are not persuasive.

It is urged, in page 13 of the remarks, that Yamazaki never discloses a difference in height from the substrate between the top surface position of said element isolating insulating film and the top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film. However, as shown in the fig. 8F of Yamazaki, a difference in height from the substrate [101] between the top surface position of said element isolating insulating film [110] and the top surface position of said semiconductor layer [103] is at least three times as large as the thickness of said gate insulating film [118].

It is urged, in pages 13-14 of the remarks, that the bottom of film [110] is not a trench because the oxide layer [110] is formed on the epitaxial layer, and subsequently into the epitaxial layer, no part of the epitaxial layer is removed to form a trench of any kind. However, it is not necessary for a part of the epitaxial layer is removed to form a trench. Since any surface that is formed below a top surface of a layer can create a trench in the layer, Yamazaki shows a trench structure. It is also urged that Yamazaki

specifically uses LOCOS to provide isolation, and does not use shallow trench isolation. Since the oxide film [110] is formed in a shallow trench, it is considered as a shallow trench isolation.

It is urged, in page 14 of the remarks, that trenches [112] of Yamazaki include a BPSG film 115c, which might be argued to correspond to the claimed "element isolating insulating film". However, as mentioned in the rejection, the oxide layer [110] (not the BPSG film [115c]) is considered as the element isolating insulating film.

Since claim 2 recited limitations similar to those recited in claim 1, claim 2 is still rejected by Yamazaki.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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April 16, 2005